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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/657,898
Filing Date: September 09, 2003
Appellant(s): STEINECKE ET AL.

Yonghong Chen
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/03/06 appealing from the Office action mailed 07/25/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 5,949,098	MORI	09-1999
US 6,696,712	YONESAKA	02-2004
US 6,825,553	CHUA ET AL.	11-2004
US 2002/0145915 (cited for evidence)	OGURA ET AL.	10-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1-3 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US. 5,949,098) in view of Yonesaka (US. 6,696,712).

Regarding claims 1 and 6, Mori (Fig. 3) discloses an electronic device, comprising: a semiconductor chip (column 2, lines 7-9); the semiconductor chip having a plurality of metallization layers 370/350/330/310 and a plurality of insulation layers 360/340/320 configured alternately one above another on the active top side; the plurality of metallization layers including topmost metallization layers having a plurality of voltage supply structures 310/330/350 (column 4, lines 39-53) and lower metallization layers disposed underneath the topmost metallization layers and having a plurality of signal line structures 371/372/373 (column 5, lines 1-6); the plurality of insulation layers 360/340/320 formed with a plurality of passage contacts 321/341/361 connecting the plurality of voltage supply structures or the plurality of signal line structures to the contact areas; the topmost metallization layers 350/330/310 having ones of the plurality of passage contacts 321/341/361 connected to the contact areas; the topmost

metallization layers 350/330/310 having at least a first one of the plurality of voltage supply structures 332 for a ground or low supply potential and a second one of the plurality of voltage supply structures 331 for a power or high supply potential (column 5, lines 40-49); the first one of the plurality of voltage supply structures 332 being insulated from the second one of the plurality of voltage supply structures 331; the first one of the plurality of voltage supply structures 332 of the topmost metallization layers 350/330/310 having a grid of supply interconnect 332 configured parallel to one another (see interconnects 332 in metallization layer 330), the second one of the plurality of voltage supply structures 331 of the topmost metallization layers 350/330/310 having a grid of supply interconnects 331 configured parallel to one another (see interconnects 331 arranged in metallization layer 330); and the grid of supply interconnects 332 of the first one of the plurality of voltage supply structures being rotated parallel relative to the grid of supply interconnects 331 of the second one of the plurality of voltage supply structures; wherein the supply interconnects 332 of the grid of the first one of the plurality of voltage structures 332 all have a ground supply potential that is different from the power supply potential of the supply interconnects 331 of the grid of the second one of the plurality of voltage supply structures 331.

Mori does not disclose that the semiconductor chip having active topside with a plurality of contact areas.

However, Yonesaka (Fig. 2) teaches the forming of a semiconductor chip having active topside with a plurality of contact areas 3a-3e, and the forming of the plurality of insulation layers formed with a plurality of passage contacts connecting the plurality of

metallization layers to the plurality of contact areas 3a-3e of the active topside. Accordingly, it would have been obvious to provide o an active top side of the semiconductor chip of Mori with a plurality of contact areas in order to provide the electrical contacts of the voltage supply lines/signal lines to the circuits formed in the substrate of the semiconductor chip, as taught by Yonesaka (see Fig. 2 and column 5, lines 56-63).

Regarding claim 2, Mori further discloses that the semiconductor chip includes an integrated circuit subdivided into a plurality of functional module regions 421 and 422 (see Fig. 4), and each one of the plurality of module regions 421 and 422 has a plurality of passage contacts connecting one of the plurality of contact areas to the first one of the plurality of voltage supply structures 332 and to the second one of the plurality of voltage supply structures 331 (see Fig. 3).

Regarding claim 3, as discussed in details above, the combination of Mori and Yonesaka substantially reads on the interconnect structures and the electrical connections as claimed. Yonesaka (Fig. 2) further teaches that the semiconductor chip having an integrated circuit formed near the active topside of the semiconductor substrate 1. The combination of Mori and Yonesaka does not teach that the electrical connections are wired using place-route programs.

However, it would have been obvious to use place-route programs for wiring the electrical connections because this wiring technology is well known and commonly use for providing the arrangement of the electrical connections in each of the metallization planes of the integrated circuit (see "Background" of Applicant's invention, page 2)..

Regarding claim 7, Mori (Fig. 3) further discloses that ones of the plurality of insulation layers located between the topmost metallization layers 350/330/310 have a thickness dimensioned to provide an electrical capacitance c31/c32/c33 that is as high as possible with sufficient dielectric strength at areas of the topmost metallization layers that are configured one above another (column 5, lines 40-49).

Regarding claims 8-9, it would have been obvious to form the plurality of metallization layers and the insulation layers of Mori with the materials as claimed because such metallization materials (i.e., aluminum, copper) and insulation materials (i.e., silicon dioxide, silicon nitride) are well known and commonly used for providing the electrical interconnections and insulations in the interconnect structures.

Regarding claim 10, Mori (Fig. 6) further discloses that the supply interconnects of the grid of the first one of the plurality of voltage supply structures 613/614 have a thickness and a width that are greater than the thickness and the width of the interconnects of the plurality of signal line structures 651/652, and the supply interconnects of the grid of the second one of the plurality of voltage supply structures 611/612 have a thickness and the width that are greater than the thickness and the width of the interconnects of the plurality of signal line structures 651/652.

2. Claims 11-13 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US. 5,949,098) in view of Yonesaka (US. 6,696,712) and Chua et al (US. 6,825,553).

Regarding claims 11 and 16, as discussed in details above (see ground of

rejection of claims 1 and 6 above), the combination of Mori and Yonesaka substantially reads on the above claims, including the forming of a plurality of module regions 421 and 422 configured below the topmost metallization layers (see Mori, Figs. 3-4).

Neither Mori nor Yonesaka disclose a semiconductor wafer having a plurality of semiconductor chip positions configured in rows and columns.

However, Chua (Fig. 4) teaches the forming of a semiconductor wafer having semiconductor chip positions 406 configured in rows and columns. Accordingly, it would have been obvious to form a plurality of semiconductor chip positions of Mori configured in rows and columns on a semiconductor wafer because the forming of chips on the wafer is well known and commonly used in the semiconductor wafer technology for forming a plurality of semiconductor chips at a same time, as taught by Chua (column 8, lines 44-60).

Regarding claim 12, , Mori further discloses that the semiconductor chip includes an integrated circuit subdivided into a plurality of functional module regions 421 and 422 (see Fig. 4), and each one of the plurality of module regions 421 and 422 has a plurality of passage contacts connecting one of the plurality of contact areas to the first one of the plurality of voltage supply structures 332 and to the second one of the plurality of voltage supply structures 331 (see Fig. 3).

Regarding claim 13, as discussed in details above, the combination of Mori and Yonesaka substantially reads on the interconnect structures and the electrical connections as claimed. Yonesaka (Fig. 2) further teaches that the semiconductor chip having an integrated circuit formed near the active topside of the semiconductor

substrate 1. The combination of Mori and Yonesaka does not teach that the electrical connections are wired using place-route programs.

However, it would have been obvious to use place-route programs for wiring the electrical connections because this wiring technology is well known and commonly use for providing the arrangement of the electrical connections in each of the metallization planes of the integrated circuit (see "Background" of Applicant's invention, page 2)..

Regarding claim 17, Mori (Fig. 3) further discloses that ones of the plurality of insulation layers located between the topmost metallization layers 350/330/310 have a thickness dimensioned to provide an electrical capacitance c31/c32/c33 that is as high as possible with sufficient dielectric strength at areas of the topmost metallization layers that are configured one above another (column 5, lines 40-49).

(10) Response to Argument

Issue No. I: Claims 1-3 and 6-10 as being unpatentable over Mori in view of Yonesaka under 35 U.S.C. 103(a).

The examiner has stated that Fig. 3 of Mori (see below) clearly discloses "said grid of supply interconnects of said first one of said plurality of voltage supply structures **being rotated relative to** said grid of supply interconnects of said second one of said plurality of voltage supply structures". Specifically, Fig. 3 of Mori clearly discloses the grid of supply interconnects 332 (i.e., ground) of the first one of the plurality of voltage supply structures being rotated parallel relative to the grid of supply interconnects 331 (i.e., power) of the second one of the plurality of voltage supply structures.

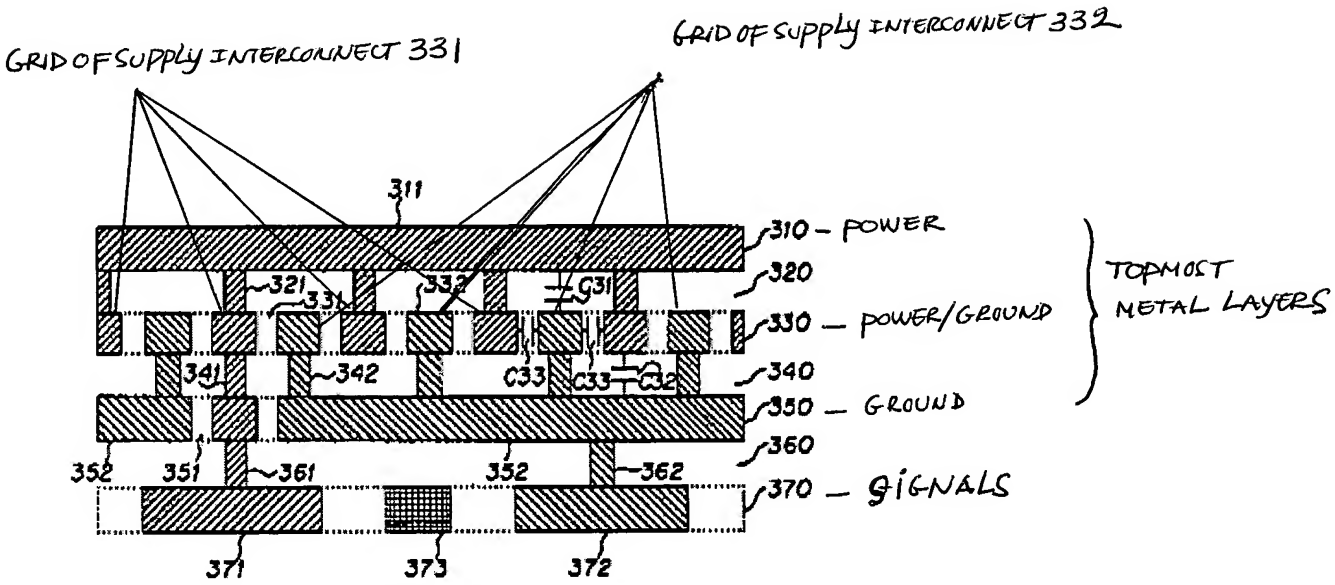

FIG. 3

However, Appellant (pages 7-9 of Brief) argues that Mori does not suggest the grid of supply interconnects of the first one of the plurality of voltage supply structures "being rotated relative to" the grid of supply interconnects of the second one of the plurality of voltage supply structures because Appellant asserts that the term "being rotated relative to" must be meant that the two grids of supply interconnects must be oriented orthogonally as shown in Fig. 4 of the instant application, but not oriented parallel as asserted by the examiner.

This argument is not persuasive because of the following reasons:

First, the feature of having two grids of supply interconnects being rotated orthogonally relative to each other as relied by Appellant does not seem to be required by the claim language because it is not stated in the claims. It is the claims that define

the claimed invention, and it is claims, not specifications that are anticipated or unpatentable. *Constant v. Advanced Micro-Devices Inc.*, 7 USPQ 2d 1064.

Second, Appellant is reminded that claims in a pending application should be given their broadest reasonable interpretation. *In re Pearson*, 494 F. 2d 1399, 181 USPQ 641 (CCPA 1974). In this case, the claim language does not specifically recite how the grid of one supply interconnects "being rotated" relative to the grid of other supply interconnects. Therefore, the phrase "being rotated relative to" can be interpreted as "being rotated relative to" any orientation, including parallel orientation. Thus, Mori does suggest the invention as claimed because Mori's Fig. 3 discloses the grid of supply interconnects 332 "being rotated" or oriented parallel relative to the grid of supply interconnects 331. And

Third, the U.S. Publication No. 2002/0145915, issued to Ogura et al, is cited to provide the evidence that a person of ordinary skill in the art would understand that the term "being rotated relative to" can be interpreted as "being rotated relative to" any orientation, including parallel orientation of the two interconnect lines. Specifically, Figs. 3A and 3B of Ogura discloses a plurality of interconnect lines being connected to the source regions 321 and the drain regions 322 to form the source lines and bit lines D0 – D3, "the source lines are **rotated to run parallel to** the bit lines" (column 1, par. [0004], lines 6-7). Therefore, "parallel" orientation can be considered to be covered under the term "being rotated relative to" in its broadest interpretation.

Issue No. II : Claims 11-13 and 16-17 as being unpatentable over Mori in view of Yonesaka and Chua et al under 35 U.S.C. 103(a).

Appellant (pages 9-10 of Brief) again argues that Fig. 3 of Mori does not suggest the grid of supply interconnects of the first one of the plurality of voltage supply structures "being rotated relative to" the grid of supply interconnects of the second one of the plurality of voltage supply structures as claimed in base claim 11.

This argument again is not persuasive because Fig. 3 of Mori clearly discloses the grid of supply interconnects 332 (i.e., ground) of the first one of the plurality of voltage supply structures being rotated parallel relative to the grid of supply interconnects 331 (i.e., power) of the second one of the plurality of voltage supply structures.

The further discussions with respect to Mori's Fig. 3 above in conjunction with **Issue No. I** are herein incorporated by reference.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

PC

May 9, 2006

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